DRAWING AMENDMENTS

All of the following changes are implemented on the attached replacement drawing sheets:

In Figure 1A, block 31 is relabeled as -- MEMORY CONTROLLER--;

In Figure 1B, block 31 is relabeled as -- MEMORY CONTROLLER CHIP--;

In Figure 1B, block 40 is relabeled as -- INTERFACE CIRCUIT--;

In Figure 2, block 31 is relabeled as -- MEMORY CONTROLLER--;

In Figure 3A, block 233 is relabeled as -- ADDR DEC--;

In Figure 3A, blocks 211 and 213 are relabeled as --MEMORY SECTOR--;

In Figure 3B, signal line 235 is relabeled as --FROM ADDRESS DECODER--;

In Figure 6, the legend of element 31 is relabeled as -- MEMORY CONTROLLER--;

In Figure 6, block 515 is relabeled as --REC & S/P--;

In Figure 7, the legend of element 31 is relabeled as -- MEMORY CONTROLLER--;

In Figure 7, block 603 is relabeled as --INTF IN--;

In Figure 11, the floating gate 1023' has been drawn as a continuous line;

In Figure 12, block 1081 is relabeled as --ROW DECODER--;

In Figure 12, block 1119 is relabeled as --ERASE DECODER--;

In Figure 13, the signal line "Serial Out" is relabeled as --1253-- and is now pointing toward block 1150;

In Figure 17A, block 1415 is relabeled as --PROGRAM DECODER--;

In Figure 17A, block 1417 is relabeled as --ERASE DECODER--;

In Figure 17A, element 1111 is relabeled as --INTERNAL ADDRESS BUS--;

In Figure 17A, floating gates have been added to the transistors in 1400 and 1420;

In Figure 17B, the control gate of 1465 has been relabeled --CLK K--;

In Figure 17B, the outputs of block 1480 have been respectively relabeled --READ BIT 1—to --READ BIT L--;

In Figure 21B, the block for ΔI_2 is relabeled as --1543--; and

In Figure 22, the memory cells 1 to n have had floating gates added.

REMARKS

Non-elected claims 63-80 have been cancelled. Duplicate claims 98 and 99 have also been cancelled. A typographical error in claim 100 is being corrected.

This response is being filed with the assumption that the claims to be pursued in this application were elected by the Response to Third Requirement for Restriction, filed December 27, 2005. Only those of claims 81-100 which read on the species A specified in the Office Action dated August 29, 2005, were elected. Therefore, when the present Office Action identifies claims 81-100, it is assumed that only those claims of that group that were elected in the Response filed December 27, 2005 are intended. However, if the Examiner intends that the election of species of the Office Action dated August 29, 2005 be withdrawn, which would be welcomed, then the withdrawn claims of the group of claims 81-100 will be restored as active claims. There is only a single independent claim 81, in any event.

Title and Abstract

The title is has been amended in accordance with the suggestion on page 2 of the Office Action. The Abstract of the Disclosure has been amended to include the requested concise statement of the technical disclosure of the subject matter being claimed.

Drawings

The drawings were objected to under 37 CFR §1.81. Substitute pages of formal drawings are being filed herewith include all the changes requested on pages 2-4 of the Office Action. A listing of the specific changes made to the drawings are provided in the Drawing Amendments section above.

Specification

The disclosure was objected to because of many alleged informalities. In response, all of the amendments requested on pages 4 and 5 of the Office Action have been made.

Claim Objections

Claims 98 and 99, objected to under 37 C.F.R. §1.75(c), have been cancelled.

Claim Rejections Under 35 U.S.C. §112

A few of the claims have been rejected under 35 U.S.C. §112, second paragraph, as being indefinite for failing to particularly point out and distinctly claim the subject matter regarded to be the invention.

With regard to claim 81, it is being amended to make clear that it is the memory cells of the blocks that are reset. Erasure of the memory cells is an example of resetting them. The objection to "a chunk of user data" is believed remedied by amending claim 96 to use the definite article in front of that phrase. The grounds of rejection of claim 81 are thus believed to be overcome.

The rejection of claim 87 is not understood, however. It seems clear in reciting that the spare cells "within a particular block" are used within "said particular block" in place of any defective cells within the block's "said plurality of cells." The "said plurality of cells" finds antecedent in claim 81, namely those memory cells into which the chunk of data is being programmed. What claim 87 says is that if any of these "plurality of cells" are defective, spare cells in the same block of memory cells are substituted.

The rejection of claim 89 is also not understood. The specification describes the cache buffer 705 of Figure 8, for example, to temporarily store a data file that is to be written into the memory. Individual chunks of these data are programmed into the memory in parallel.

Nothing indefinite can be found about claims 91 and 97. The recitation that the claimed method is being carried out on a single integrated circuit chip appears to be a precise statement.

Claim 92 is being amended to use language that the Examiner should find acceptable.

The general objection to claim 100, without providing any specific basis for it, cannot be responded to. Claim 100 is, however, being amended to better match the antecedents in claim 81.

Double Patenting Rejection

Certain claims stand rejected on the ground of non-statutory obviousness-type double patenting as being unpatentable over specific claims of United States patent no. 5,991,517 to Harari et al. (" '517 "). In order to facilitate prosecution of the present application, a Terminal

Disclaimer is being filed herewith without taking a position whether such a Disclaimer is necessary or not.

Claims 81-86, 88-90, 92-96 and 98-100 also stand rejected on the ground of non-statutory obviousness-type double patenting as being unpatentable over claims 1-10 of United States patent no. 6,914,846 to Harari et al. (" '846 "). This rejection is, however, respectfully traversed. Claims 1-10 of this patent define techniques for erasing multiple units of memory cells together. The present application claims define methods of programming data. The two sets of claims really have no relationship with each other.

Information Disclosure Statement

It is noted that the Examiner has considered all references submitted in Information Disclosure Statements dated July 26, 2006 and November 22, 2006. References submitted in a Supplemental Information Disclosure Statement dated December 9, 2003, which were also resubmitted via a Request to Enter Previously Filed Third Supplemental Information Disclosure Statement filed October 2, 2006, remain unacknowledged. This document, as well as the cited references, are available in PAIR. It is respectfully requested that this Supplemental Information Disclosure Statement be considered and the PTO Form 1449 be initialed and returned with the next Action.

Conclusion

Accordingly, it is believed that this application is now in condition for allowance and an early indication of its allowance is solicited. However, if the Examiner has any further matters

that need to be resolved, a telephone call to the undersigned at 415-318-1163 would be appreciated.

FILED VIA EFS

Respectfully submitted,

Gerald P. Parsons — Date 4/3/07
Reg. No. 24,486

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